

#14/S-10-C4
B/v Jones



PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

Takaki YOSHIDA et al.

Group Art Unit: 2133

Serial No.: 09/697,305

Examiner: Joseph D. Torres

Filed: October 27, 2000

For: FAULT DETECTING METHOD AND LAYOUT METHOD
FOR SEMICONDUCTOR INTEGRATED CIRCUIT

RECEIVED

AMENDMENT

MAY 05 2004

Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

Technology Center 2100

Sir:

Prior to examination of the above-identified continuing application, please amend the claims in the application as follows: